

REMARKS

After the foregoing Amendment, Claims 1-7 and 16 are currently pending in this application. Claims 8-15 have been canceled without prejudice. Claims 1 and 16 have been amended to clarify the language used therein. Applicants submit that no new matter has been introduced into the application by these amendments.

Claim Rejections - 35 USC §103

Claims 1, 2, 4, 5, 7 and 16 stand rejected under 35 USC §103 as being unpatentable over U.S. Patent No. 7,194,011 B1 (Nassiri-Toussi et al., hereinafter referred to as Nassiri) in view of U.S. Patent No. 7,173,992 B2 (hereinafter referred to as Frigon) and U.S. Patent Application Publication No. 2003/0119444 A1 (hereinafter referred to as Yamaguchi). The Applicants respectfully disagree.

The claims as amended are related to a method and apparatus for performing initial cell search. The method comprises processing to detect a peak primary synchronization code (PSC) location (i.e. chip offset or chip location), obtaining a t_{offset} and code group, and identifying the preamble of a base station with which the WTRU performing the initial cell search may synchronize with.

Nassiri discloses a method for performing pipelined cell searches and reducing the number of false lock conditions in a communication system. Frigon discloses a method for synchronization in wireless systems using receive diversity.

Yamaguchi discloses a method for cell search synchronization using primary and secondary synchronization codes with symbol partitioning.

With respect to Claim 1, Nassiri, Frigon, and Yamaguchi do not teach or suggest, either alone or in any combination, the feature of decoding the selected SCH signal to determine system time frame timing and base station identity by determining a beginning of the SCH signal by identifying a chip location having a highest signal to noise ratio wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame. Further, Applicants could not find any teaching receiving an identifying synchronization channel (SCH) signal from at least one base station at a predetermined chip rate in a selected portion of a system time frame in Nassari, Frigon, or Yamaguchi. Lastly, Applicants could not find where the feature of identifying received SCH signals using a power threshold is disclosed, taught, or suggested in Nassir, Frigon, or Yamaguchi.

Claims 2-7 are dependent either directly or indirectly upon patentable amended independent Claim 1, which the Applicants believe are allowable over the cited prior art of record for the at least same reasons as patentable amended independent Claim 1.

With respect to Claim 16, Nassiri, Frigon, and Yamaguchi do not teach or suggest, either alone or in any combination, at least one correlator configured to

identify received SCH signals using a power threshold based on a plurality of chip samples sampled at twice the chip rate. Further, Nassiri, Frigon, and Yamaguchi do not teach or suggest, either alone or in any combination, a processor configured to decode a selected SCH signal to determine system time frame timing and base station identity by determining a beginning of the SCH signal by identifying a chip location having a highest signal to noise ratio wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame.

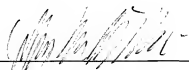
Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1 – 7 and 16, is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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Enclosures